ELEC 3004/7312: Signals Systems & Controls

Prac/Lab 1: Introduction to the NEXYS 2 + Sampling & Reconstruction on the NEXYS 2

Revised March 17, 2013

Pre-Lab

Note: The tutors will *not* assist you further unless there is real evidence you have attempted questions prior to the tutorial.

This laboratory is the combination of what used to be two sessions. This is now laboratory session with two experiments (i.e., Introduction to the NEXYS 2 and Sampling & Reconstruction on the NEXYS 2).

The Pre-laboratory exercise for this laboratory is to :

- Read through Experiments I and II of the Laboratory 1 Guide
- Read through the Experiment I Preparation
- **Read and Complete Experiment II Preparation (page 14)**

Laboratory Completion & Extra Credit Points

Доверяй, но проверяй

(doveryai, no proveryai – "*Trust, but verify*")

Laboratory Completion:

Please work **together** on the lab in groups of 2-3. Please submit an **individual** hand-in sheet. Treat the questions at the end of the Experiments as thought questions – questions that you should be able to answer, but not that you have to answer explicitly. Though you could be asked these during a tutor group review.

Tutor Group Review:

At various stages in the lab (or at the end) the tutors will come around to check progress. The **may** ask some questions to check your understanding. Each person in the group **may** get asked different questions at the tutor's discretion. Based on your answers they will mark (initial) your hand-in sheet. The tutors are just checking that you understand the core ideas of each Experiment and its Parts.

Extra Credit Points:

This practical laboratory is worth 1-4 Extra Credit Points on the final exam.
These will be distributed based on completion (as determined by the head tutor for your practical session) of the following sections at the end of the practical session.

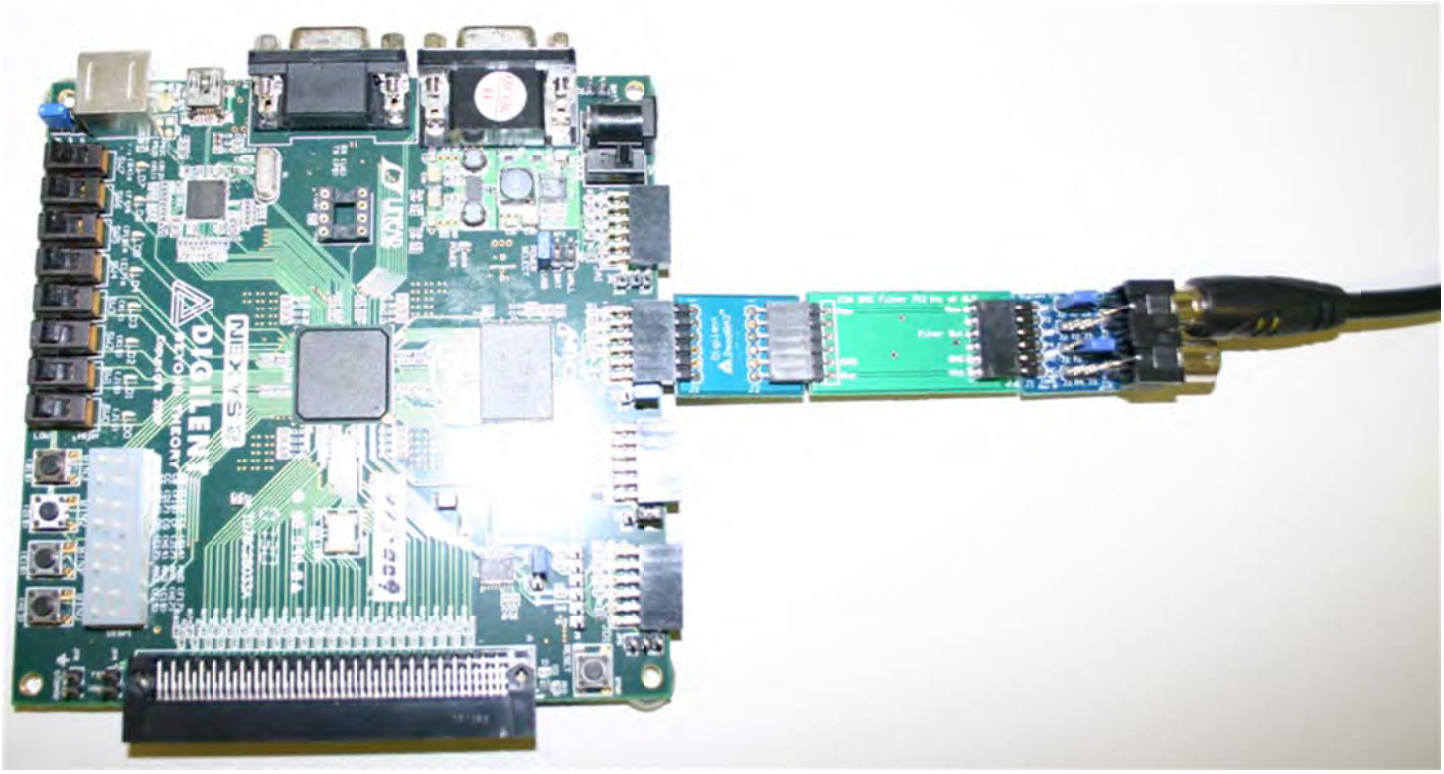
Section Completed	Total Points Extra Credit Earned
Pre-Lab (Preparation for Lab 1 – Experiment II – p. 14)	+ 1
Complete Experiment I	+ 2
Complete Experiment II – Part 1 & 2	+ 3
Complete Experiment II – Part 3	+ 4

Experiment I: An Introduction to the NEXYS 2

Digilent's Nexys 2 is a **field programmable gate array** (FPGA) development board that allows for rapid and interactive implementation and debugging of FPGA designs. The Nexys2 provides communications to and from the FPGA, plus access to a wide range of peripherals such as LCD, RAM, serial flash memory, and analogue to digital/**digital to analogue converters** (ADC/**DAC**) via IO ports. This **e**xperiment focuses on the **DAC** interfaces, which are available in 8-bit as well as 12-bit versions.

Equipment

1. PC with Xilinx ISE 13.4, Digilent Adept & MATLAB;
2. Nexys 2 + USB to JTAG interface cable/s
3. Digilent PMOD-DA2 DAC board and PMOD-CON4 RCA board
4. Oscilloscope
5. 2 x cable: RCA male to BNC male approx 0.5 - 1 m
6. 1 x E36 DAC Filter board (UQ designed)



Preparation

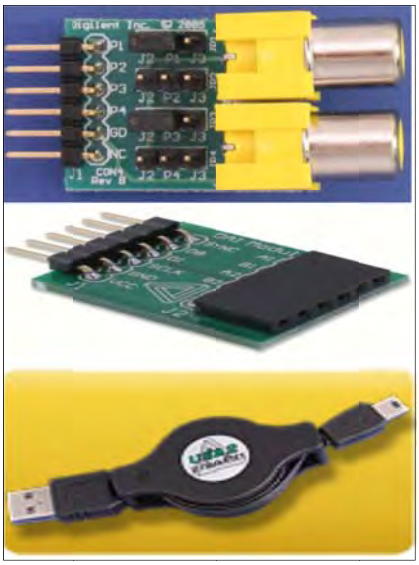
Read and familiarise yourself with the following documents available from the course (or manufacturer's) website:

- The Nexys 2 Reference Manual Pages 1-5, 15, 17; http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,789&Prod=NEXYS2
- Digilent PMOD interface boards: http://www.digilentinc.com/Products/Catalog.cfm?NavPath=2,401&Cat=9
- PMOD DA2 Dual 12-bit DAC http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,401,487&Prod=PMOD-DA2
- PMOD AD1 Dual 12-bit ADC http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,401,499&Prod=PMOD-AD1

Answer the following questions:

1. Tabulate the two's complement binary representation of the decimal numbers -8 to 7. How many bits are required to do this? Identify the "sign bit" and the most significant bit.
2. Tabulate the unsigned binary representation of the decimal numbers 0 to 15. If this binary representation is then "shifted" (i.e., AC coupled) so that 0 represents $-V_{DD}/2$ and 15 represents $+V_{DD}/2$, again, identify the "sign bit" and the most significant bit.
3. Given the PMOD-AD1 can handle a range of input levels from GND to V_{DD} (where V_{DD} = 5v) and it has a 12-bit, unipolar binary analogue to digital (ADC), what is the quantisation step-size of the ADC?
4. The PMOD-DA2 is a 12-bit unipolar DAC with an output range from GND to VDD (where V_{DD} = 5v). What is the quantisation step-size of its output?
5. Can you explain how the code in SINEWAVE.VHD generates a sine wave? Can you predict the effect of increasing the number of samples in the LUT?
6. For 12-bit unsigned binary, what are the maximum and minimum decimal values?
7. Convert the minimum and maximum values, as well as 2048, 2831 and 3495 to hexadecimal, then into 12-bit binary. What are the values of I (index) for these values in the Look-up-table in the appendix?

Nexys 2 FPGA Board



PMOD-CON4, PMOD-DA2, USB-JTAG

DAC Filter board

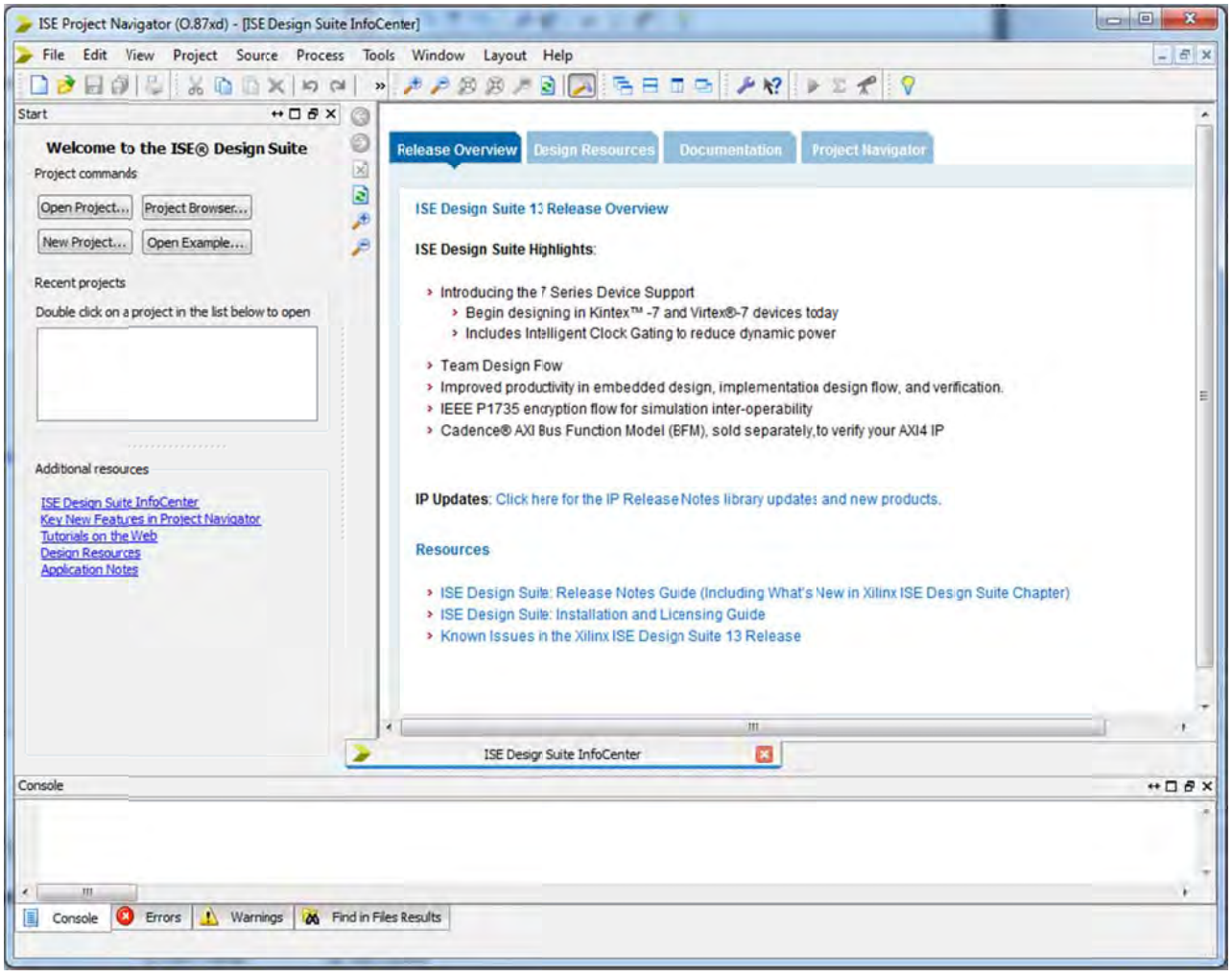
Procedure

Part 1: Getting familiar with the Nexys 2 by generating a sine wave

1. Start Xilinx ISE using the desktop icon or run C:\Xilinx\13.4\ISE_DS\ISE\bin\nt64\ise.exe

Assemble the Nexys2 Board with a PMOD-CON4 (RCA), DAC Filter Board and PMOD-DA2 attached to JB1, as shown on page 1.

Now connect an RCA/BNC cable between the PMOD-CON4 upper socket and CH 1 on the oscilloscope**, then connect a second cable from the lower PMOD-CON4 socket to CH 2 on the oscilloscope.**



2. Create an FPGA Project

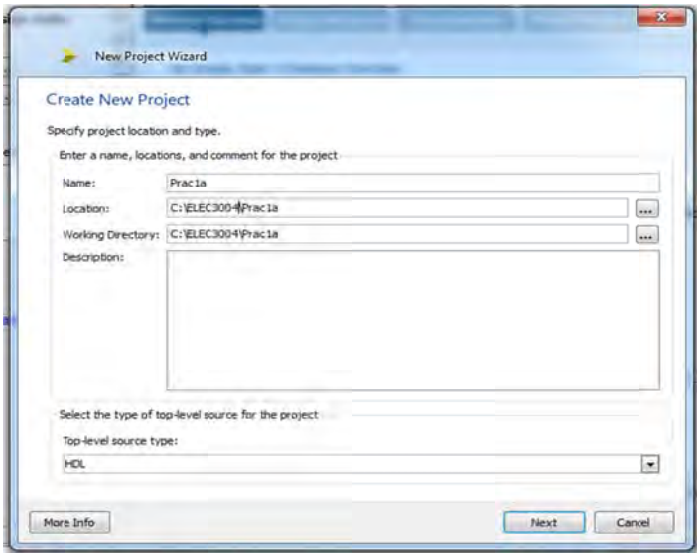
3. Click on "**New Project**".

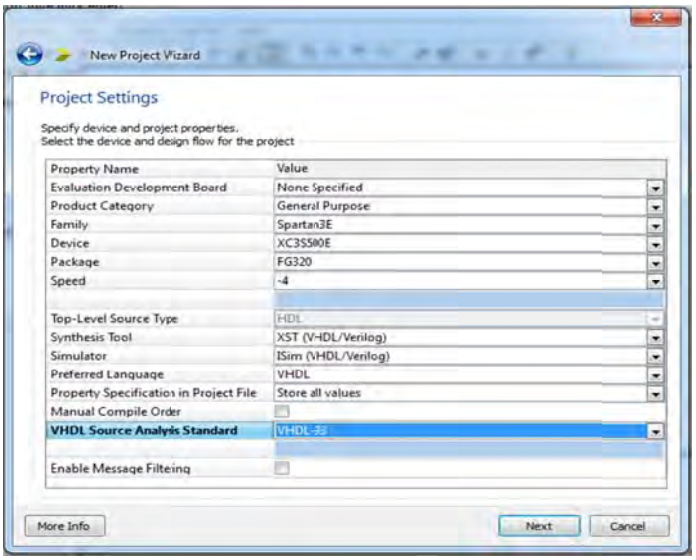
4. Type in the Location or Working Directory, then the Name of your Project.

If you use a network drive, this will significantly slow things down, so use a local drive or USB drive!

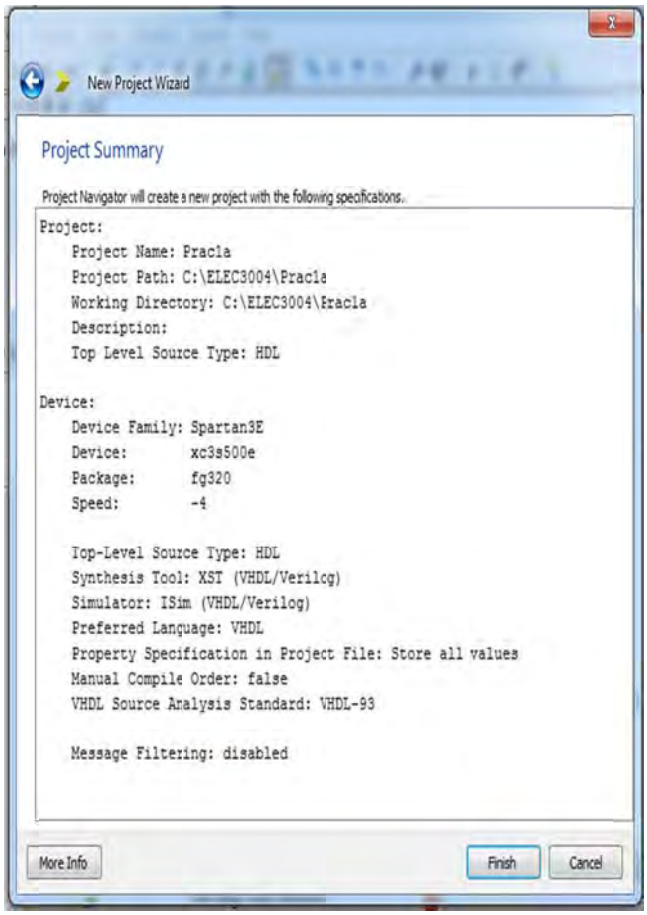
You may have to use the Browse Directory button [**...**]

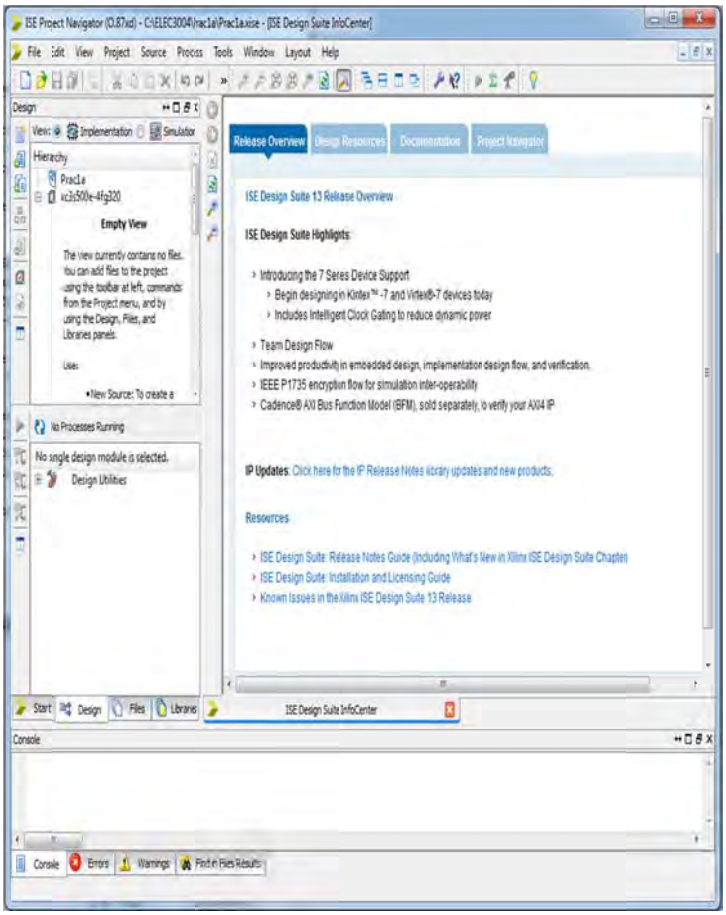
Enter the Device Properties as shown: General Purpose, Spartan 3E, XC3S500E, FG320, -4, HDL, XST, ISIM, VHDL





5. You will now see a Project Summary page. Click “Finish” The files for your project can now be added



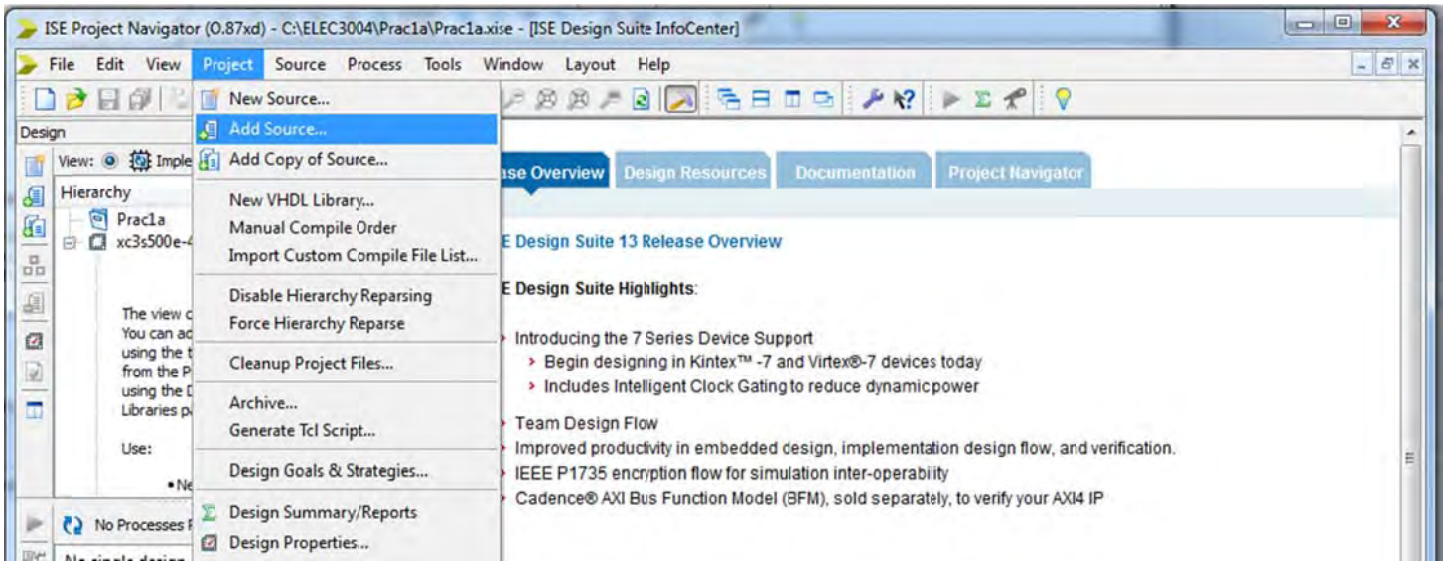


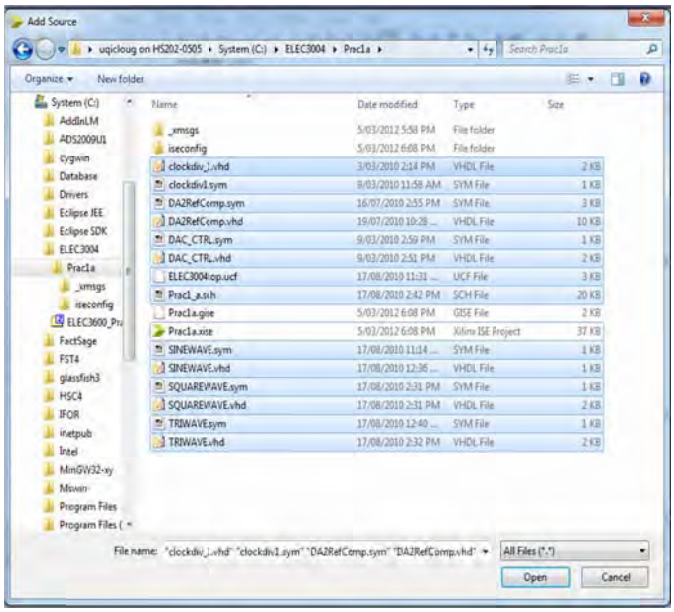
6. Download the following files from the ELEC3004 website and place them in your Working Directory:

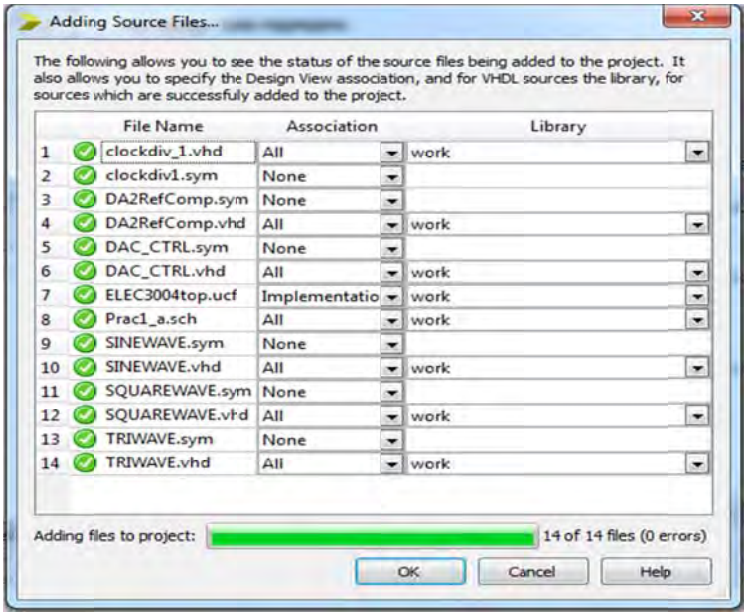
sinewave.vhd
clockdiv_1.vhd
DAC_CTRL.vhd
DA2RefComp.vhd
squarewave.vhd
triwave.vhd
Prac1_a.sch
clockdiv1.sym
SINEWAVE.sym
DA2RefComp.sym
DAC_CTRL.sym
squarewave.sym
triwave.sym
ELEC3004top.ucf

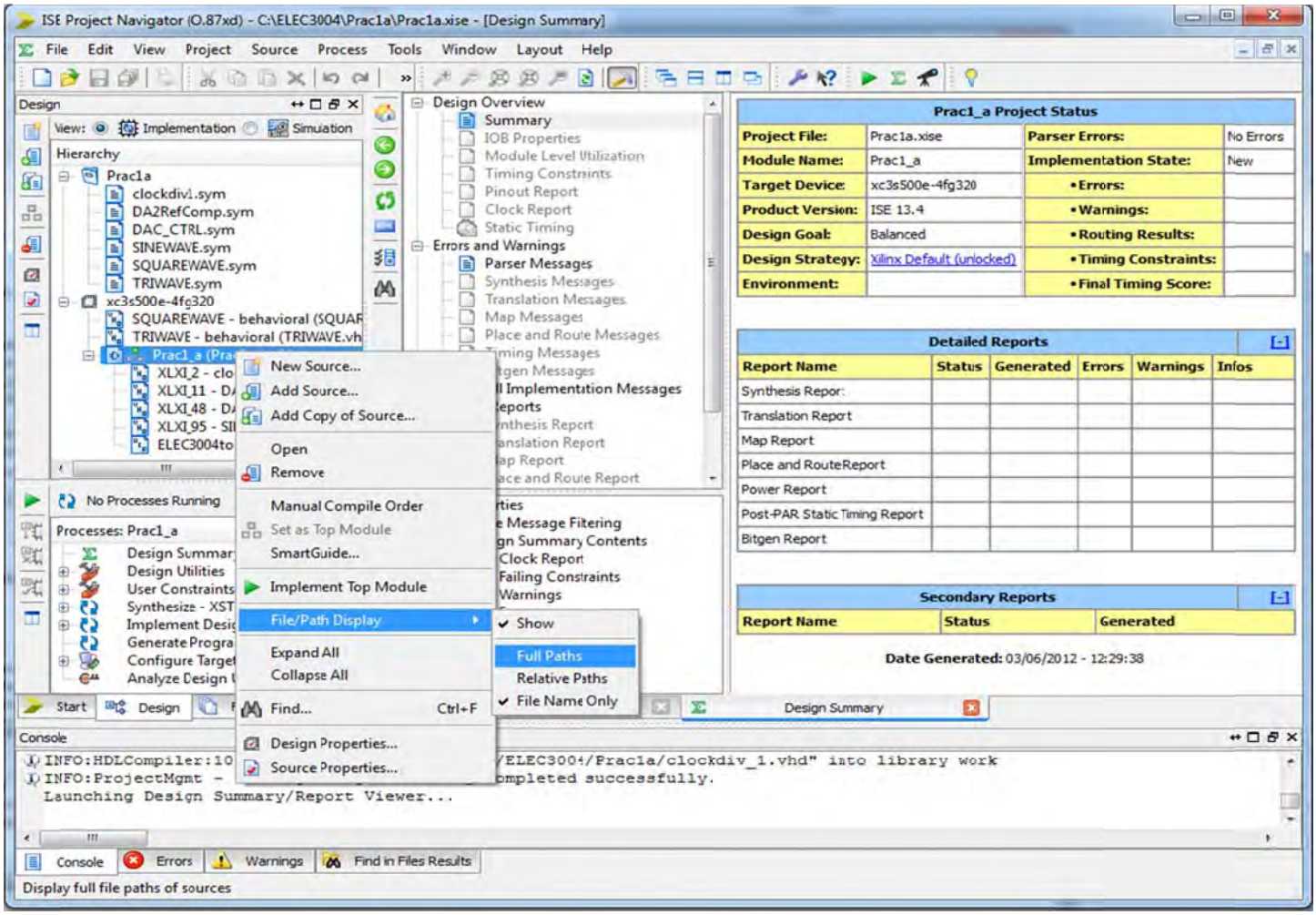
These may also be available in a zip file -- http://robotics.itee.uq.edu.au/~elec3004/labs/Lab1Files.zip

7. Now use **Project\Add Source** and add all the files.



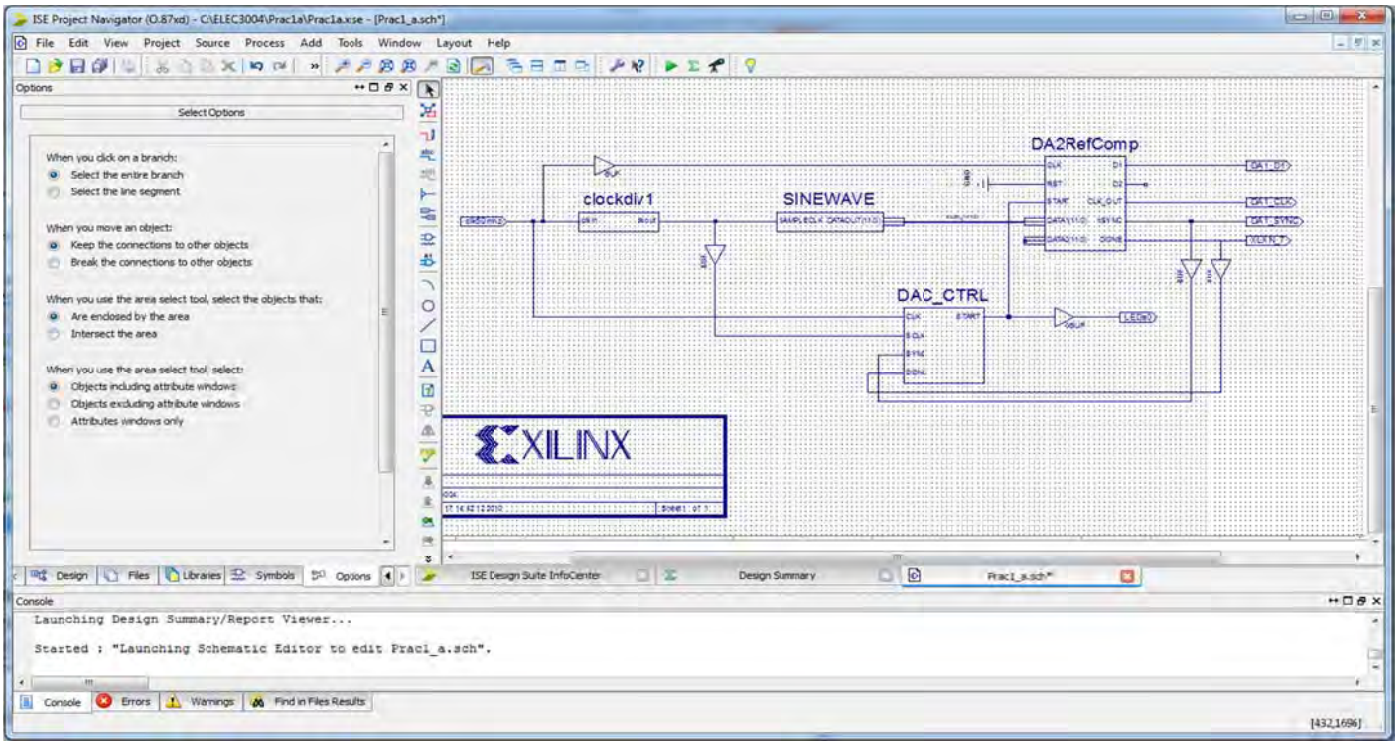




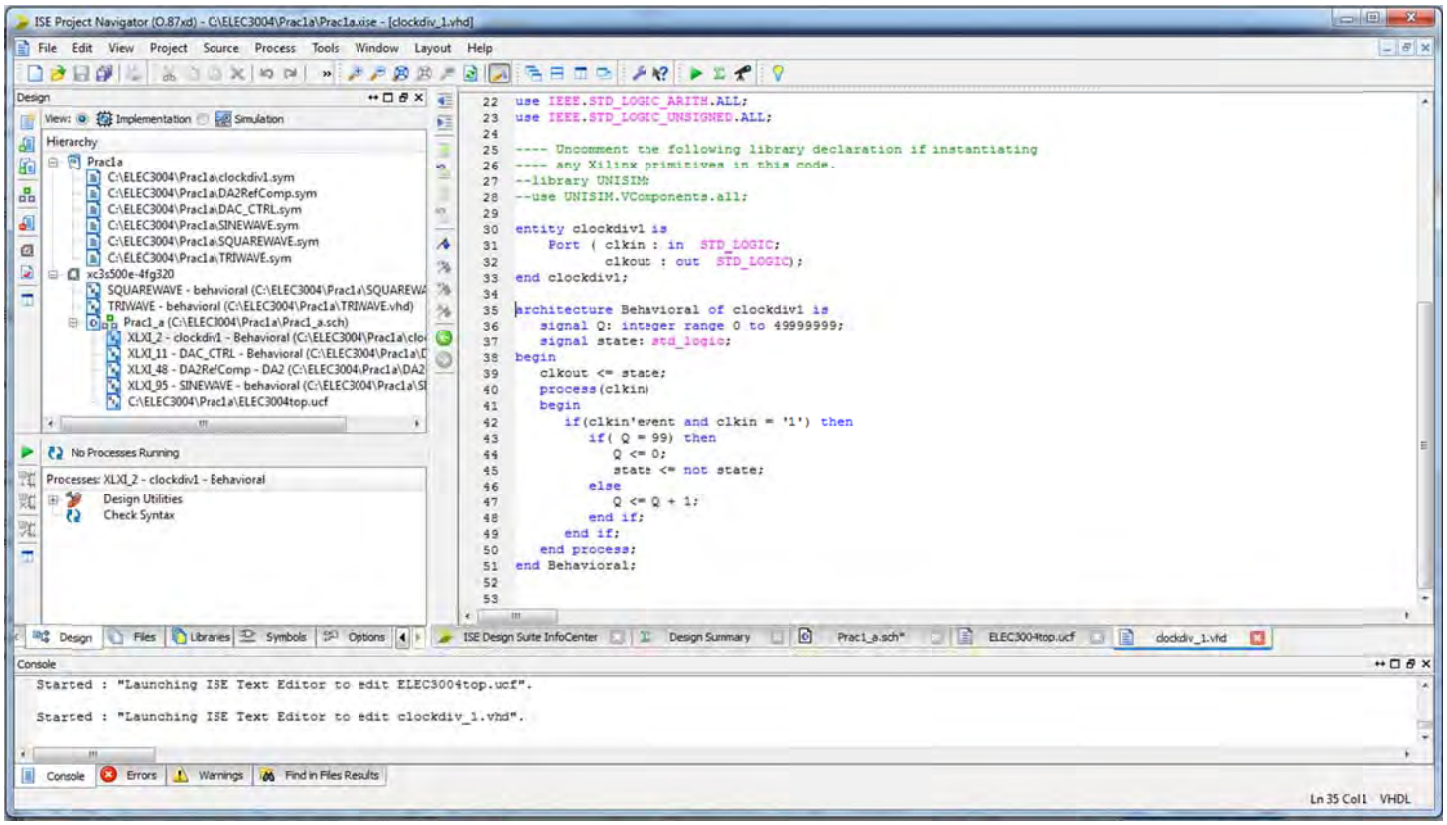


8. **Set the Full Paths option as shown above**

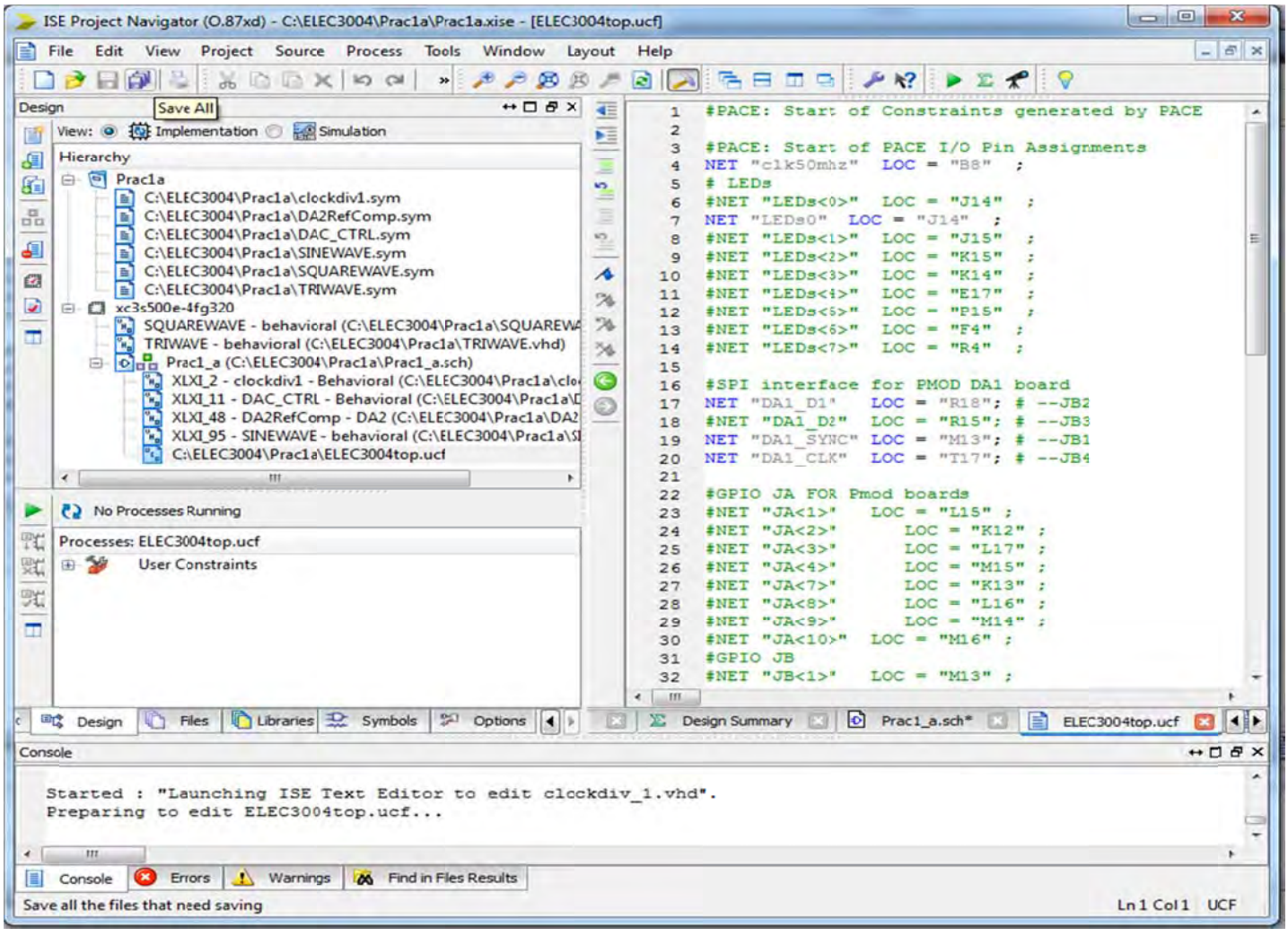
9. **If you double-click on Prac1_a.sch, it will open in a window in the Project View Window:**



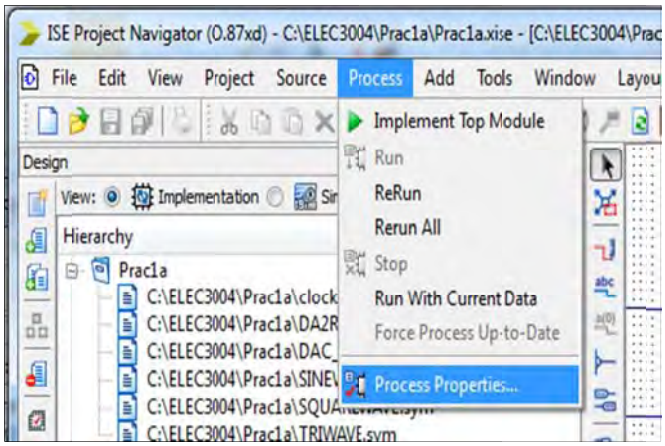
10. 10.If you double-click on any of the ".vhd" files, you will see the contents of that file in the Project View window

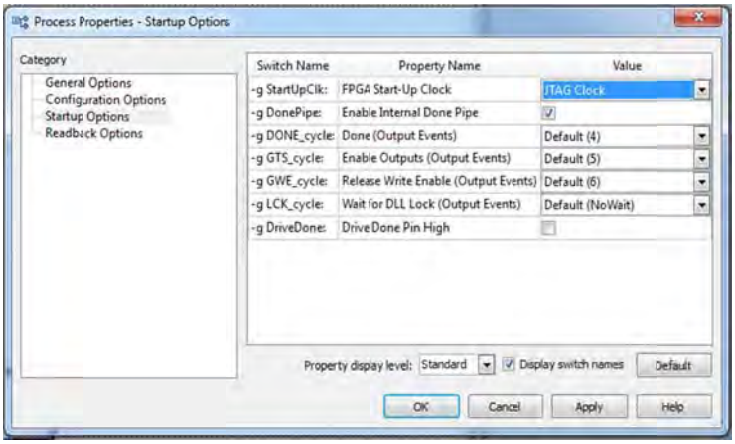


11. To see the contents of ELEC3004top.ucf, double-click on the filename



12. Next select **Process Properties**, then in Startup Options, set **FPGA Start-Up Clock** to JTAG Clock, and then click OK. ***If this is the first time you have used this software, you may have to try instruction 13 below, first, then repeat instruction 12 to set the FPGA Start-Up Clock.***



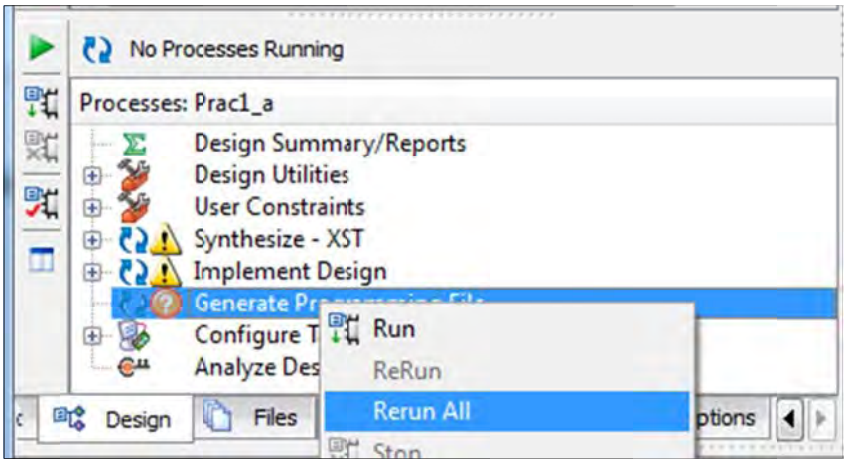


Now you can generate the file which will be downloaded to the Nexys 2 board using Digilent Adept software.

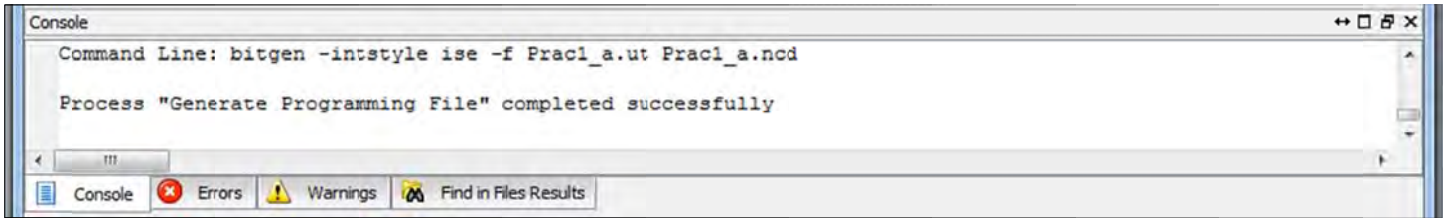
13. **Click once** on the Prac1_a filename in Hierarchy, and then double-click **Generate Programming File**.

If necessary, repeat instruction 12 to set the FPGA Start-Up Clock.

After 1 - 2 minutes, a file called “prac1_a.bit” will be saved to your Working Directory



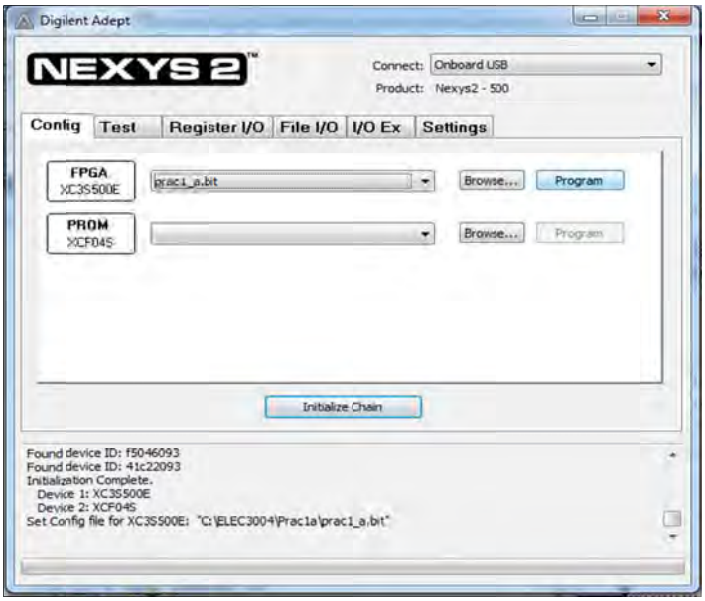
If all has gone well, you will see a message, “**Process "Generate Programming File" completed successfully**” in the Console window at the bottom of the screen.

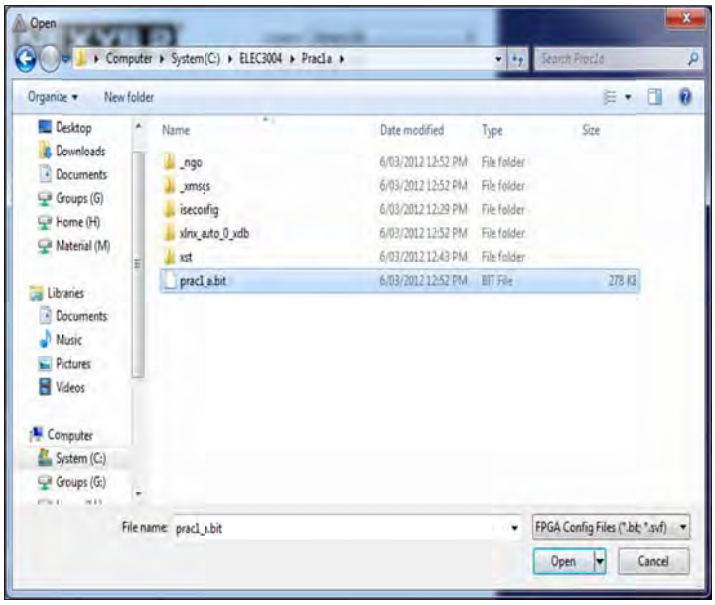


Using the Digilent Adept software

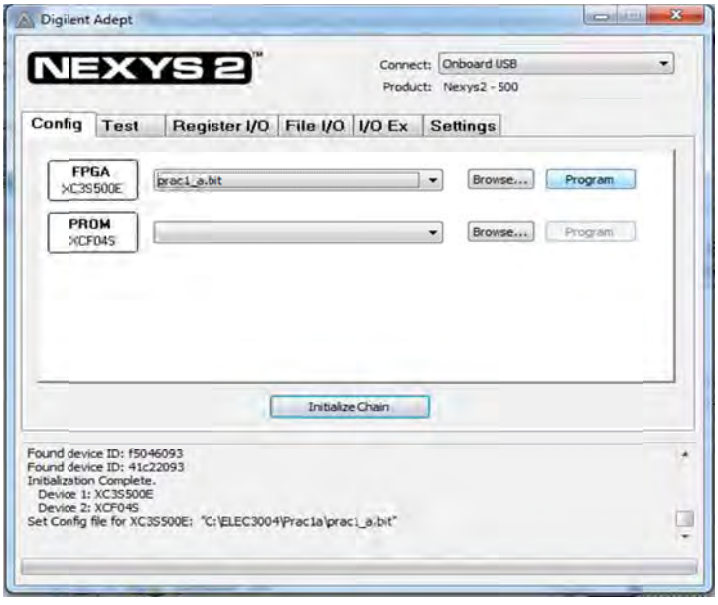
1. To download the file to your board, connect the USB to JTAG cable that comes with the Nexys 2 board, then start up the Digilent Adept software.

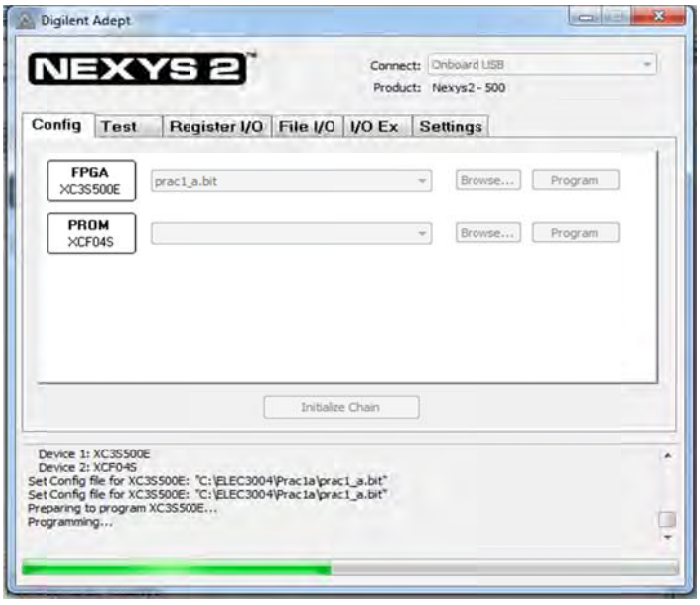
2. From the startup page, you may have to select Onboard USB, then Browse to your file and select Open





3. Now press the **Program** button. A green progress bar will appear





4. You should now have a sinewave being sent to the PMOD-DA2 on port JB1 of the Nexys 2. You may look at this with your oscilloscope to verify that it is working correctly. To see the VHDL code used to generate the sinewave, double-click on the SINEWAVE.VHD file.

Thought Questions

If you have the DAC Filter board available, the Raw signal is connected to the upper PMOD-CON4 connector and the Filtered signal is connected to the lower PMOD-CON4 connector.

Plot the output waveform/s on the oscilloscope. What is the amplitude and frequency of the sine wave generated on each available channel?

The Master Clock is 50MHz, which is then divided by 200, in clockdiv1.vhd, to produce **Fr**. This frequency, **Fr**, controls the readout rate of the LUT which is n=16 elements long. If it takes 16 clock cycles of **Fr** to produce a complete LUT cycle, what is the theoretical audio output frequency? Is it the same as your measured frequency?

Try to confirm that the DAC step size is approximately the same as that calculated in the preparation. If it is not, can you explain why? **Hint** 1: is the DAC connected directly to the output? **Hint** 2: can you see a relationship between the steps in the output waveform, and the changes in the values in the LUT?

Suggest how you might modify the VHDL code so that a LUT with only 8 points is required. What are the advantages and disadvantages of this approach?

Appendix – Part 1:

Sinewave.vhd

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity SINEWAVE is port
   (
        DATAOUT      : out  std_logic_vector(11 downto 0);
        SAMPLECLK    : in   std_logic
   );
end SINEWAVE;


architecture behavioral of SINEWAVE is

signal I : integer range 0 to 15;

begin
            with I select
         DATAOUT <= "100000000000" when 0,     --800
                    "101100001111" when 1,     --B0F
                    "110110100111" when 2,
                    "111101100011" when 3,
                    "111111111111" when 4,
                    "111101100011" when 5,
                    "110110100111" when 6,
                    "101100001111" when 7,
                    "100000000000" when 8,
                    "010011110000" when 9,
                    "001001011000" when 10,
                    "000010011100" when 11,
                    "000000000000" when 12,
                    "000010011100" when 13,
                    "001001011000" when 14,
                    "010011110000" when 15;

            I <= I + 1 when rising_edge(SAMPLECLK);
   end behavioral;
```

END PART I

Experiment II: Sampling & Reconstruction on the NEXYS 2

Aims

In this laboratory section you will:

- Gain familiarity with the workings of an audio codec on the Nexys 2;
- Gain practical experience of the sampling and reconstruction of analogue signals, in particular you will characterise the anti-aliasing and reconstruction filters and observe the effects of aliasing;

Introduction

The Digilent Nexys 2 provides an FPGA-based **codec** and DSP system, where the functionality is implemented in VHDL, a **H**ardware **D**escription **L**anguage, rather than in conventional software. This implementation uses a **schematic** approach, so that the experimenter can see the structure of the DSP system graphically, then view and modify as necessary, the contents of the relevant modules in the system.

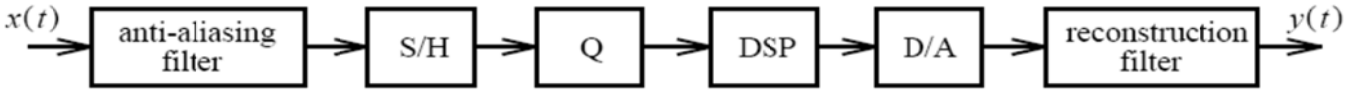


Figure 1: A block diagram of a practical DSP system.

Figure 1 shows a block diagram of a typical digital signal processing (DSP) system. On the Nexys 2 the ADC has a low pass filter with nominal cut-off frequency of around 500 kHz, however additional 10 kHz lowpass filters can be inserted at input and output. The Nexys 2 codec is implemented as separate analogue to digital (A2D) and digital to analogue (D2A) converters, these being represented by the sample and hold (S/H) plus quantiser (Q) and D/A blocks in Figure 1 respectively. Finally, the DSP block in Figure 1 is where the difference equation for implementing the desired digital filter is performed.

Equipment

PC with Xilinx ISE , Digilent Adept & Matlab;

1. PMOD AD1 and DA2 boards
2. 2 x PMOD CON4 boards
3. ADC and DAC Filter boards
4. Nexys 2 + JTAG interface cable/s;
5. Oscilloscope (preferably with FFT function);
6. 2 x cable: mono RCA male to mono BNC male, 0.5 - 1 metre long
7. Mono or stereo 3.5mm male to mono or stereo RCA male
8. Mono or stereo Y-adaptor, 3.5mm Male to 2 x 3.5mm Female
9. Signal Generator;
10. External speakers + audio jack cable + power pack;
11. 1 BNC T-adaptor M to 2F (F-M-F);
12. 1 x cable BNC Male to BNC Male, 0.5 - 1 metre long.

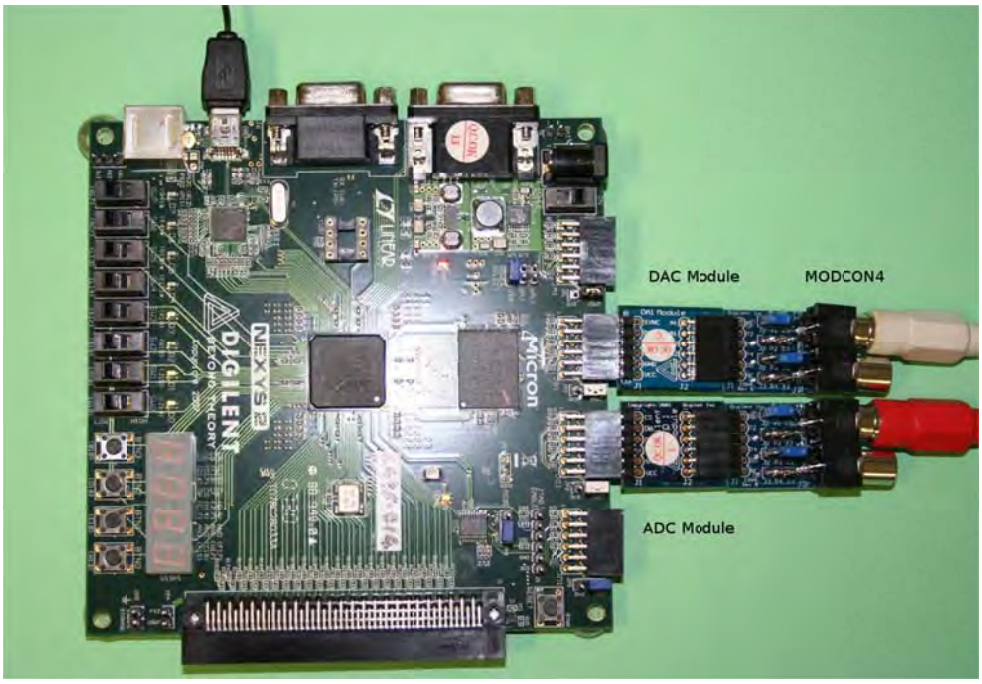


Figure 2. Nexys2 board with cable connections

Preparation

Note: preparation will be checked at the start of each laboratory class.

Answer the following questions:

1. Bearing in mind that the anti-aliasing filter on the PMOD-AD1 is set to approx. 500kHz, explain what happens to the analogue signal, x(t), after it has passed through this filter and is presented to the input of the A2D, when:
   - x(t) is a sinusoidal signal of frequency 10 kHz;
   - x(t) is a square wave (50% duty cycle) of fundamental frequency 4 kHz.

2. What is the Fourier series representation of a square wave and of a triangle wave?

3. If the DSP block in Figure 1 is assumed to have a sampling frequency of 25 kHz and performs the following difference equation: y[n] = x[n], (that is, the output of the A2D is copied directly to the input of the D2A) what is the frequency and approximate amplitude of the signal, y(t), observed at the **output** of the reconstruction filter, when:
   - x(t) is a sinusoidal signal of frequency 10 kHz;
   - x(t) is a sinusoidal signal of frequency 12.5 kHz;
   - x(t) is a sinusoidal signal of frequency 15 kHz;
   - x(t) is a square wave of fundamental frequency 4 kHz;

4. Assume a 2^{nd} order Sallen-Key lowpass filter with corner frequency (F_c) of 10 kHz is used for the anti-aliasing and reconstruction filters.
   - What is the expected attenuation at F_c?
   - What is the cutoff slope in dB/octave and dB/decade?

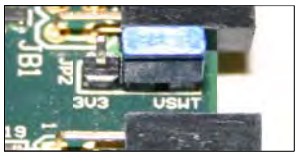
Procedure

Part 1: Sampling and Reconstruction

With reference to EXPERIMENT 1: INTRODUCTION TO THE Nexys2, carry out the following:

Start Xilinx ISE and Digilent Adept

8. Connect PMOD DA2 to JB1, and connect PMOD AD1 to JC1, both on the top row, then connect a PMOD CON4 to each, so that your connection looks like figure 2 above.



9. Ensure that JP2 and JP3 (near JB1 and JC**1**) have jumper blocks connecting the centre pin and VSWT.
10. Using an appropriate cable and T-piece combination, connect the output of the signal generator via the T-piece, to PMOD AD1 and to channel 1 of the oscilloscope.
11. Connect the output of PMOD DA2 to channel 2 of the oscilloscope.
12. Set CH1 and CH2 of oscilloscope to **DC Coupling** from the CH1/CH2 Menu buttons
13. On the function generator, pull the **Offset** button out and set the **Amplitude** control counter-clockwise and select **SINE** wave.
14. Open the FPGA Project: **Prac2_Part1_2012.xise**
15. Open **Prac2_Part1_2012.sch** and **codec.vhd** file by double clicking on these file names.
16. **Ensure that slide switch 0 (SW0) is set to 0, i.e. down, or nearest the edge of the board.**

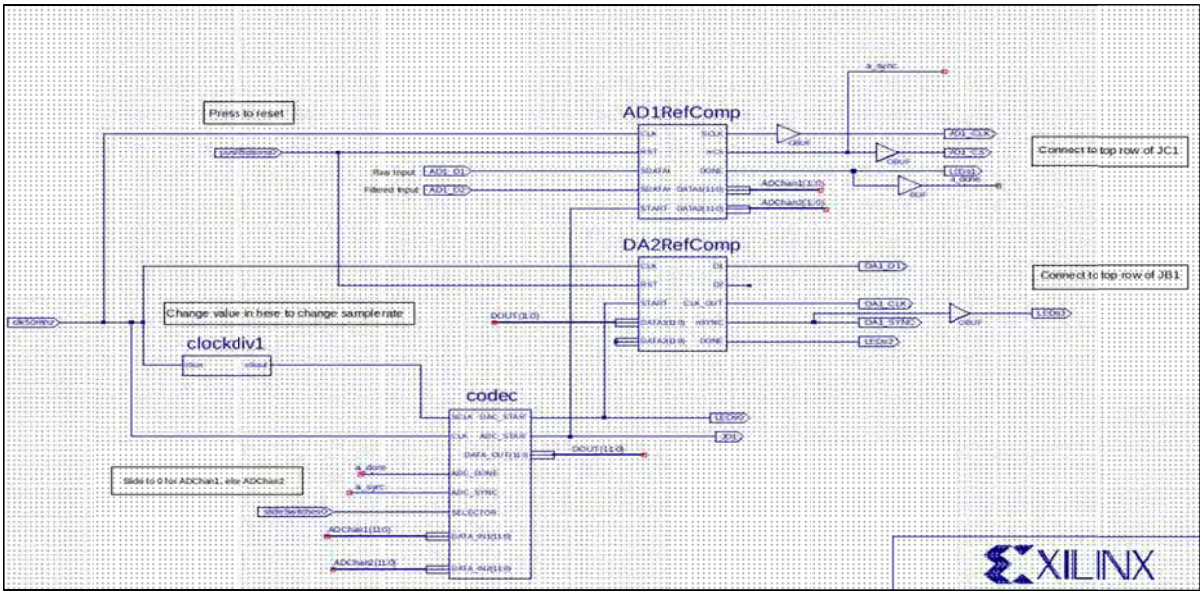


Figure 3. Sample and Reconstruct schematic

17. In the Design View select **Generate Programming File | ReRun All** and wait until the bitfile is produced.
18. Download it to the Nexys2 board using Adept.
19. You will need to experiment with offset voltage and amplitude (**Page 3**) on the signal generator. Suitable starting values would be approx 2.5 volts DC for **Offset**, then **Amplitude** of approx. 4.5 Vp-p.

Part 2: Tasks and questions

Please ensure you adjust your input so that the output signal is sinusoidal, not clipped or distorted.

For the phase response, just record the time difference (in uS) between input and output signal.

This section does not use the filter boards.

Use the signal generator to plot the magnitude and phase response, H(ω), of the system (i.e., from x(t), the input, through to y(t), the output) between DC and 12 kHz. To do this it is suggested that you make measurements at (at least) the following frequencies: 0.125, 0.25, 0.5, 1, 2, 4, 6, 8, 10, and 12 kHz;

1. What components of the block diagram in Figure 1 are contributing to your measured H(ω)?
2. Is your measured phase response linear? Should it be?
3. Do your measurements confirm your answer to preparation question 1 (a)? If not, why?

7. Now slowly increase the frequency of the input sine wave, x(t), from 10 to 15 kHz.

1. What happens to the frequency of the output sine wave, y(t)?
2. Explain what is happening in terms of the Nyquist rate and the sampling theorem;
3. Do your measurements confirm your answer to preparation question 2 (a), (b) and (c)?
4. What happens to the frequency of the output sine wave, y(t), when the input sine wave, x(t), approaches 25 kHz? That is, when x(t) is equal to the sampling frequency.

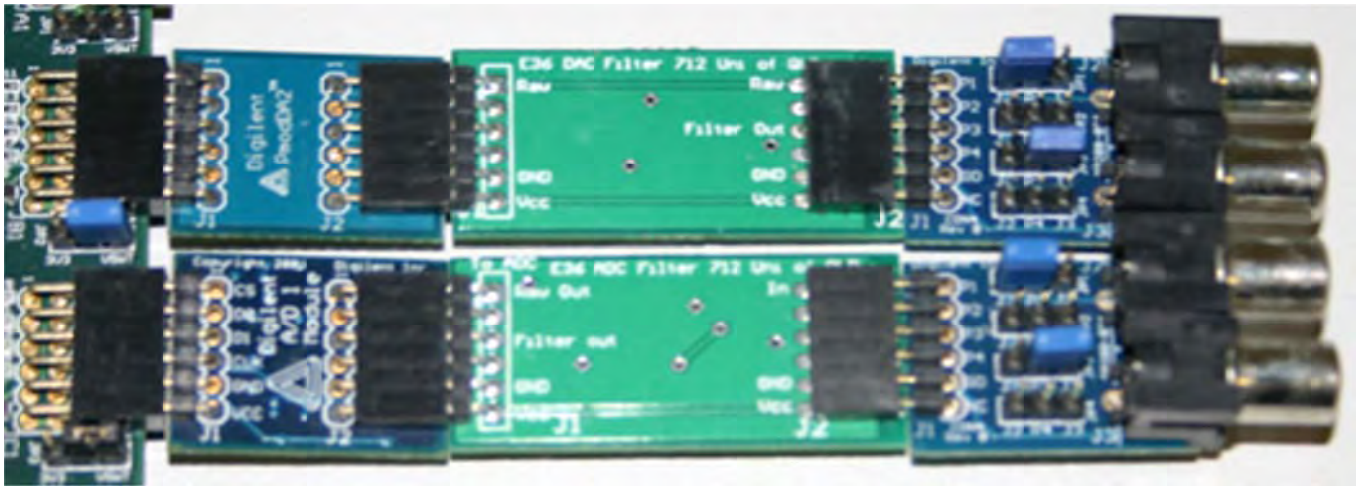
8. Set up the function generator to produce a **square** wave. Observe the audio output on the CRO both in the time and frequency domain (*using the FFT function from the MATH menu*).

1. What distortions do you observe in the audio output as you vary the fundamental frequency of the square wave from 100 Hz to 12 kHz? i.e., as compared to spectrum of the audio input.
2. Do your measurements confirm your answer to preparation question 2 (d)?
3. How can these distortions be explained? i.e., which components of Figure 1 are causing them? And what effect is aliasing having? Is your input signal amplitude too high?
4. Observe the time difference between the square wave input and the reconstructed output. How does the time difference change as you vary the frequency from 0 to 4 kHz?
5. What is the cause?

Part 3 :Tasks and questions

This section USES the filter boards.

Fit the DAC filter between the DA2 board and its CON4 board. Fit the ADC filter between the AD1 board and its CON4 board.



If you look at the schematics in the appendix, you will see that there are connections for Raw Out and Filtered Out. This allows you to experiment with various combinations of input and output signals, being:

1. Raw in, Raw out
2. Raw in, Filtered out
3. Filtered in, Raw out
4. Filtered in, Filtered out.

Slide switch 0, **SW0**, allows you to select raw In (0), or Filtered In (1) for the ADC. The DAC filter board has Raw Out on the top connector and Filtered Out on the bottom connector. Combination a) is the same as not having the filter boards at all.

Part 3 continued:

If you move SW0, you can select between a) and c) for the top connector (Raw Out), and between b) and d) for the bottom connector (Filtered Out).

Remember to keep the input pk-pk value under 5V.

Connect the function generator to CH1 of the oscilloscope and the ADC.
Set the function generator to Sinewave, 5 V p-p and DC offset of 2.5 volts.

For the following data, plot this in a spreadsheet and show to a tutor.

1. Connect the Raw Out (top connector) to CH2.

Raw in – Raw out

- Move SW0 to 0 (Raw in) then sweep the frequency from about 100Hz to about 25 kHz and observe the output on CH2. Record the input and output amplitudes, plus Frequency Out at 1, 4, 10, 15 and 20 kHz.

Filtered in – Raw out

- Now move SW0 to 1 (Filtered In) and repeat.

- Now connect Filtered out (bottom connector) to CH2.

Raw in – Filtered out

- Move SW0 to 0 (Raw in) then sweep the frequency from about 100Hz to about 25 kHz and observe the output on CH2. Record the input and output amplitudes, plus Frequency Out at 1, 4, 10, 15 and 20 kHz.

Filtered in – Filtered out

- Now move SW0 to 1 (Filtered In) and repeat.

Set the function generator to squarewave and repeat 1 to 6.

Record the results in the tables below or in a spreadsheet.

Either printout your plots, or save the files to your network drive for later review.

Data Entry Table

Sinewave Filtered in – Raw out (SW0 = 1)

Frequency in (kHz)	Vin pk-pk	Vout pk-pk	Frequency out
1			
4			
10			
15			
20			

Sinewave Raw in – Filtered out (SW0 = 0)

Frequency in (kHz)	Vin pk-pk	Vout pk-pk	Frequency out
1			
4			
10			
15			
20			

Sinewave Filtered in – Filtered out (SW0 = 1)

Frequency in (kHz)	Vin pk-pk	Vout pk-pk	Frequency out
1			
4			
10			
15			
20			

Squarewave Raw in – Raw out (SW0 = 0)

Frequency in (kHz)	Vin pk-pk	Vout pk-pk	Frequency out
1			
4			
10			
15			
20			

Squarewave Filtered in – Raw out (SW0 = 1)

Frequency in (kHz)	Vin pk-pk	Vout pk-pk	Frequency out
1			
4			
10			
15			
20			

Squarewave Raw in – Filtered out (SW0 = 0)

Frequency in (kHz)	Vin pk-pk	Vout pk-pk	Frequency out
1			
4			
10			
15			
20			

Squarewave Filtered in – Filtered out (SW0 = 1)

Frequency in (kHz)	Vin pk-pk	Vout pk-pk	Frequency out
1			
4			
10			
15			
20			

Appendix – Part 2:

Schematic diagrams for filter boards:

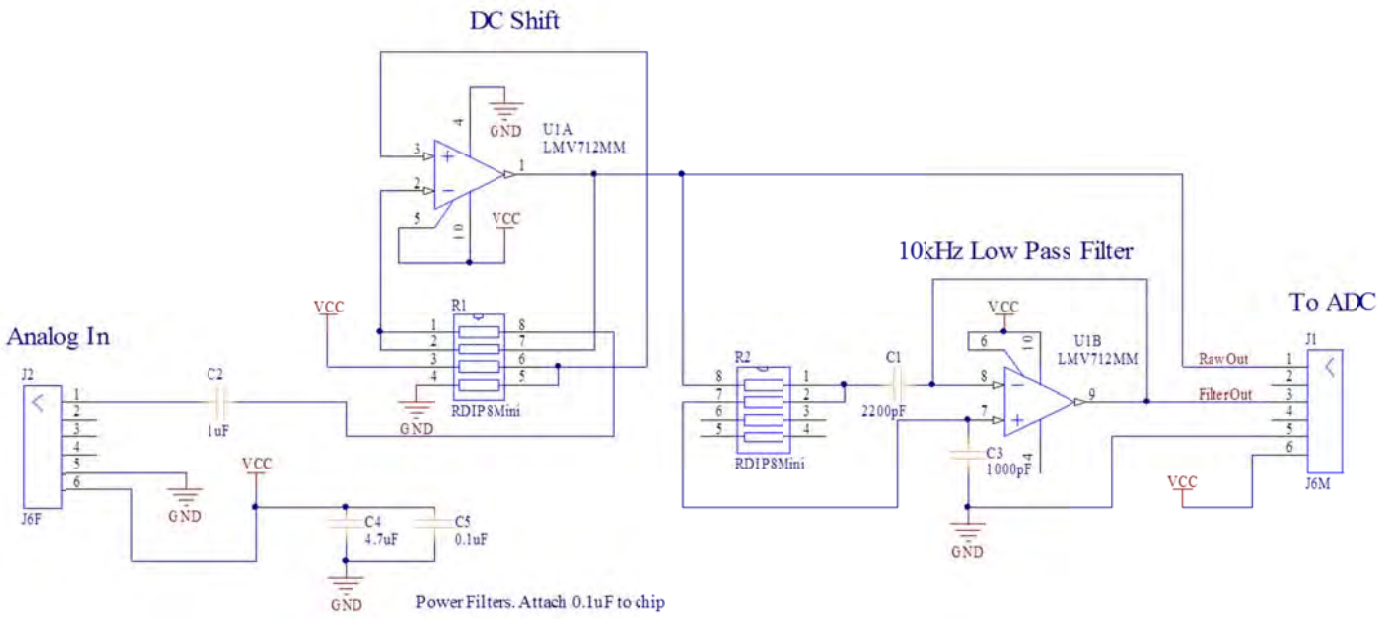


Figure 4: ADC lowpass filter

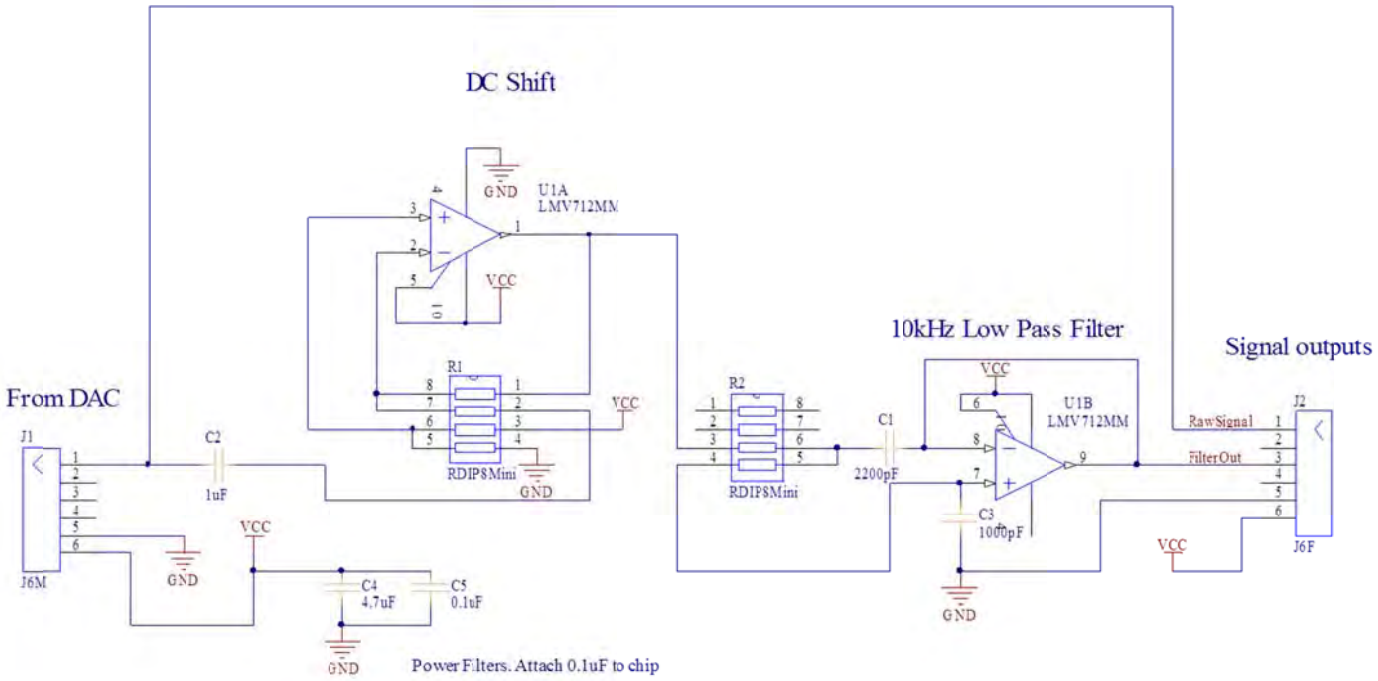


Figure 5: DAC lowpass filter

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Experiment 1:

Hand-In Sheet

Introduction to the NEXYS 2 + Sampling & Reconstruction on the NEXYS 2

Name: _____
Student ID: _____
Date: _____

Group Name/Members: _____
_____

As noted, this practical laboratory is worth 1-4 Extra Credit Points on the final exam. These will be distributed based on completion (as determined by the head tutor for your practical session) of the following sections at the end of the practical session.

Section Completed	**Summary Comments** (Student)	✓ (Tutor)
Pre-Lab (Preparation Lab 1 – Section II)		
Complete Experiment I		
Complete Experiment II – Part 1 & 2		
Complete Experiment II – Part 3		

➲ **Continued on Page 22**

Please succinctly answer the following questions for the various lab sections.

Section I

Q1) Suggest how you might modify the VHDL code so that a LUT with only 8 points is required. What are the advantages and disadvantages of this approach? List two of each. What is one overall benefit and downside to using a LUT?

Section II

Q2) Use this space to write your answers to the following questions from Part II:

a) Should the phase response be linear? Why or why not?

b) Explain, in terms of the Nyquist rate and sampling theory, what happens to the frequency of the output wave when the input wave frequency is swept from 10 to 15 kHz.

Section III

Q3) Summarise the differences between the four combinations of input and output signals experimented with in Part III. Note any differences between the sine wave and square wave outputs with the different combinations and provide a brief explanation.

Total Extra Credit Awarded: _____

Tutor Sign-Off: _____